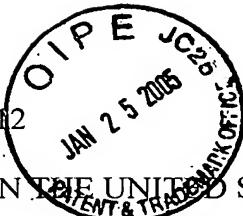


GK-US035112



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :  
Kwyro LEE et al. : Patent Art Unit: 2817  
Serial No.: 10/633,589 : Examiner: Steven J Mottola  
Filed: August 5, 2003 :  
For: VARIABLE GAIN LOW NOISE :  
AMPLIFIER :  
:

**SUBMISSION OF SUBSTITUTE SPECIFICATION**

Assistant Commissioner of Patents  
Washington, DC 20231

Sir:

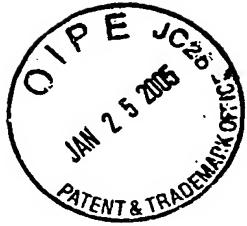
Applicant submits herewith a substitute specification, which replaces the version submitted on August 5, 2003. Applicant respectfully asserts that no new matter was added in the substitute specification. A marked copy of the original specification is also submitted herewith.

If there are any questions, please feel free to contact the undersigned.

Respectfully submitted,

  
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## VARIABLE GAIN LOW NOISE AMPLIFIER

### TECHNICAL FIELD

**[0001]** The present invention relates to a Low Noise Amplifier (hereinafter referred to as an "LNA"), more specifically, it is related to a variable gain LNA that is operated most suitably in input matching, gain and noise characteristics, linearity, etc.

### BACKGROUND OF THE INVENTION

**[0002]** A first terminal is comprised of an amplifier that generally amplifies small signals to large signals in wireless equipment, for example a portable phone, TV, etc. This amplifier is made to have an amplifying operation having low noise and high gain characteristics when the signal is very small. But linearity is demanded rather than the amplifying operation when the signal is relatively large. Therefore, the amplifier satisfies more than two kinds of amplifying modes according to the input signal level, and it is necessary that the amplifier selects one of them in the wireless frequency receiving equipment.

**[0003]** As a low noise amplifier of the prior art, it is disclosed in U.S. Pat. No 6,144,254 that it is possible to switch between a low gain and high gain state.

**[0004]** Fig. 1 shows a circuit diagram of a low noise amplifier disclosed in U. S. Patent No 6,144,254.

**[0005]** As shown in Fig. 1, the low noise amplifier comprises a common-emitter BN1 (the first NPN transistor to operate in a high gain state), common-base BN2 (the

second NPN transistor to operate in a low gain state), third NPN transistor BN3 (the third NPN transistor for provide bias current in BN2), and resistor R1.

**[0006]** That is, a collector of the first NPN transistor BN1 is connected to an output terminal Pout of an LNA, a base is connected to an input terminal Pin of an LNA and the first bias input terminal Bias1, and an emitter is grounded. The resistor R1 is connected between the first bias input terminal Bias1 and first NPN transistor BN1.

**[0007]** A collector of the second NPN transistor BN2 is connected to the output terminal Pout of the LNA, a base is connected to the second bias input terminal Bias2, and an emitter is connected to the input terminal Pin of LNA and a collector of the third NPN transistor BN3.

**[0008]** A base of BN3 is connected to the third bias input terminal Bias3, and an emitter is grounded.

**[0009]** Hereinafter an operation of the LNA of the prior art is described, referring to Fig. 1.

**[0010]** In the high gain state, the Bias1 is high, and the Bias2 and Bias3 are low. Therefore, the first NPN transistor BN1 is activated and performs the amplifying operation of a high gain, in the high state. Here, the second transistor BN2 and the third transistor BN3 are turned off.

**[0011]** In the low gain state, the Bias2 and Bias3 are high, and the Bias1 is low. Therefore, BN2 and BN3 are activated and perform the low gain amplifying operation, in the low gain state. Here, BN1 is turned off.

**[0012]** The low noise amplifier shown in Fig. 1 selects one of the states between high

gain and low gain, and then operates the high-gain or low-gain amplifying operation in accordance with the size of the received signal. But, the circuits operated for each gain state are affected by the load of the other, because input terminals of the emitter-common first NPN transistor BN1 and base-common second NPN transistor BN2 are directly connected to each other, that is the base of BN1 is directly connected to a emitter of BN2, in the low noise amplifier shown in Fig. 1. Namely, when the low noise amplifier operates in a high gain state, the capacitance of an emitter terminal of BN2 acts as a load for high gain circuits. As a result, the gain, matching, and noise characteristics of the high gain state are not good, and the capability of the low noise amplifier is reduced. In addition, when the low noise amplifier operates in the low gain state, the capability of the low gain state is reduced by the capacitance of the base terminal of BN1 in the same way as with the high gain state. Because two mode impedance levels of the input terminal are at substantially the same level, the impedances act as a load against each other.

#### SUMMARY OF THE INVENTION

**[0013]** The object of the present invention is to provide a variable gain low noise amplifier in which the circuits are designed to operate in the best suited way such that each gain mode does not affect the capability of the best suited circuit to operate in the other gain mode.

**[0014]** Another object of the present invention is to provide a variable gain low noise amplifier for which input matching, gain, noise characteristics, linearity, etc. can display the capability of the best suited circuit in different modes.

[0015] Another object of the present invention is to provide a variable gain low noise amplifier which is operated according to the size of a receiving signal in more than two amplifying modes, and can be varied between the gain in low gain modes.

[0016] Another object of the present invention is to provide a variable gain low noise amplifier whose power consumption is low.

[0017] To achieve above objects, a variable gain low noise amplifier, which amplifies the signal applied in an input terminal and outputs to an output terminal, comprises a first amplifying cell, which comprises a first terminal and second terminal connected to the output terminal, amplifies the signal applied to the first terminal to high gain, and outputs to the second terminal in high gain mode; a second amplifying cell that comprises a first terminal and second terminal connected to the output terminal, amplifies the signal applied to the first terminal to low gain, and outputs to the second terminal in a low gain mode; a selectively matching circuit that comprises a first terminal connected to the input terminal and second terminal connected to the first terminal of the first amplifying cell, and selectively changes an input impedance of the first amplifying cell; a first short-circuit means connected between the input terminal and the first terminal of the amplifying cell, and transmits the signal applied to the input terminal to the first terminal of the second amplifying cell in the operation of low gain mode; and wherein the selectively matching circuit changes the input impedance such that the power transmitted to the first amplifying cell of the signal applied to the input terminal is to be maximized in the operation of the high gain mode, and to be minimized to essentially zero in the operation of the low gain mode.

[0018] The variable gain low noise amplifier of the present invention further comprises a short-circuit means connected between the second terminal of the second amplifying cell and the output terminal.

[0019] The variable gain low noise amplifier of the present invention further comprises a short-circuit means connected between the input terminal and the output terminal.

[0020] The variable gain low noise amplifier of the present invention is provided, wherein the first amplifying cell comprises first, second, third terminals, amplifying element, resistor and degeneration impedance, and wherein the amplifying element, resistor, and degeneration impedance control the amounts of current that flow from the first terminal to the second terminal in proportion to the voltage applied to the third terminal; and a first terminal of the amplifying element is formed to connect to the second terminal of the first amplifying cell, the second terminal is connected with one of terminals of the degeneration impedance, the third terminal is connected with one of terminals of the resistor and then formed to connect to the first terminal of the first amplifying cell, the other terminal of the resistor is applied to the HG-bias voltage of activating the first amplifying cell in an operation of high gain mode, the other terminal of the degeneration impedance is grounded, and the amplifying element is connected to common mode of the second terminal.

[0021] The variable gain low noise amplifier of the present invention is provided, wherein the second amplifying cell comprises a first, second, and third terminals; a first amplifying element controls the amounts of current flowing from the first terminal

to the second terminal in proportion to the voltage applied to the third terminal; wherein the second terminal of the first amplifying element is formed to connect to the first terminal of the second amplifying cell, and the third terminal is applied to the LG-bias voltage to activate the second amplifying cell in the low gain mode operation, and the first amplifying element comprises an amplifying unit connected to common mode of the third terminal; and the second and third amplifying elements, voltage source, and variable voltage source, control the amounts of current that flow from the first terminal to the second terminal in proportion to the voltage applied to the third terminal; wherein the first terminal of the second amplifying element is formed to the second terminal of the second amplifying cell, the second terminal is connected to the first terminal of the first amplifying element of the amplifying unit by connecting with the second terminal of the third amplifying element, the third terminal is connected to one of the terminals of the voltage source, the first terminal of the third amplifying element is connected to the power source, the third terminal is connected to the variable voltage source, and the other terminals of the voltage source and variable voltage source are grounded.

**[0022]** A variable gain low noise amplifier of the present invention is provided, wherein the matching circuit comprises a first and second inductor, capacitor, and short-circuit means; and one of the terminals of the first inductor is connected with the second inductor and the capacitor, the other terminal is connected to the short-circuit means, the other terminal of the second inductor is formed of the first terminal of the matching circuit, the other terminal of the capacitor is formed to connect to the

second terminal of the matching circuit, and the other terminal of the short-circuit means is grounded.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0023] Fig. 1 shows a circuit diagram of a low noise amplifier of the prior art.

[0024] Fig. 2a shows a circuit diagram of a source-common amplifier of the prior art.

[0025] Fig. 2b shows a circuit diagram of a gate-common amplifier of the prior art.

[0026] Fig. 3 shows a circuit diagram of a variable gain LNA according to an embodiment of the present invention.

[0027] Fig. 4 shows a circuit diagram of a variable gain LNA according to another embodiment of the present invention.

[0028] Fig. 5a shows a circuit diagram of a first amplifying cell according to the present invention for the variable gain LNA shown in Fig. 3 or Fig. 4.

[0029] Fig. 5b shows a circuit diagram of a second amplifying cell according to the present invention for the variable gain LNA shown in Fig. 3 or Fig. 4.

[0030] Fig. 5c shows a circuit diagram of a selectively matching circuit according to the present invention for the variable gain LNA shown in Fig. 3 or Fig. 4.

[0031] Fig. 6a shows a circuit diagram of the variable gain low noise amplifier shown in Fig. 3 using circuits shown in Fig 5a, 5b and 5c.

[0032] Fig. 6b shows an equivalent circuit diagram of an input part of the first amplifying cell in order to describe the operation of selective matching circuits in accordance with an embodiment of the present invention, when the variable gain low noise amplifier is operated in a high gain mode.

[0033] Fig.6c shows an equivalent circuit diagram of the input part of the first amplifying cell in order to describe the operation of selective matching circuit in accordance with an embodiment of the present invention, when the variable gain low noise amplifier is operated in a low gain mode.

#### DETAILED DESCRIPTION

[0034] Hereinafter, preferred embodiments of the present invention will be described in detail with reference to the attached drawings.

[0035] Here, a common source and gate low noise amplifier of the prior art will be described, and then proper embodiments of a variable gain low noise amplifier according to present invention will be described in detail with reference to the attached drawings.

[0036] Fig 2a shows a common source amplifier of the prior art.

[0037] Referring to Fig. 2a, a common source amplifier comprises an NMOS transistor MS21, first inductor L21, second inductor L22 and third inductor L23, resistor R21 and voltage source V21. The drain of the NMOS transistor MS21 is formed to connect to an output terminal Pout connected with one of terminals of first inductor L21, the gate is connected with the resistor R21 and third inductor L23, and the source is connected with one of the terminals of the second inductor L22. The other terminal of the first inductor L21 is connected to a power source VDD, the other terminal of the second inductor L22 is grounded, and the other terminal of third inductor L23 is formed to connect to an input terminal Pin of the amplifier. The voltage source V21 is connected between the other terminal of the resistor R21 and

the ground.

[0038] The common source amplifier shown in Fig. 2a amplifies the signal applied through the input terminal Pin in a high gain mode, and can be matched to the input power and noise through a degeneration of the source. Accordingly, the source common amplifier is proper to maximize noise characteristics and gain. But, its weak point is that linearity is bad due to a voltage amplification effect caused by capacitance of the third inductor L23 and NMOS transistor MS21.

[0039] Fig. 2b shows circuit diagram of gate common amplifier of the prior art.

[0040] Shown in Fig. 2b, the gate common amplifier comprises a NMOS transistor MG21, an inductor L24, a capacitor C21, and a current source I21. The drain of the NMOS transistor MG21 is formed to connect to an output terminal Pout of the amplifier connected with one of the terminals of the inductor L24, the gate is connected to one of the terminals of the voltage source V22, and the source is connected to one of the terminals of the current source I21 and capacitor C21. The other terminal of the voltage source V22 is grounded, the other terminal of the inductor L24 is connected to the power VDD, and the other terminal of the current source I21 is grounded. The other terminal of the capacitor C21 is formed to connect to an input terminal Pin of the amplifier.

[0041] The gate common amplifier shown in Fig. 2b amplifies the signal applied through the input terminal Pin in a low gain mode. Because it cannot effect voltage amplification for use in an input matching circuit in the gate common amplifier, the gain and noise characteristics are bad compared with the source common amplifier

shown in Fig. 2a. But, it is easy to match an input resistance through the gm value by controlling of the current that flows to the NMOS transistor because the input resistance is  $1/gm$ . The value of the input resistance is much smaller than that of the source common amplifier shown in Fig. 2a. Its strong point is that the gate common amplifier can obtain a very high linearity compared to the source common amplifier, because the linearity of gm is superior in cases in which a recently developed transistor has a small channel length. And it is easy for the gate common amplifier to operate a variable gain function by means of adding a circuit to vary the output current in the output terminal of the amplifier.

**[0042]** Hereinafter describes an embodiment of a variable gain low noise amplifier (LNA) is described.

**[0043]** The variable gain LNA according to the present invention makes use of an amplification element that is a MOSFET transistor. The amplification element comprises a gate, source, and drain. The MOSFET transistor has the characteristics that allows the direction of a current flowing from the source to the drain or the other way to be decided according to the value and polarity of the voltage applied to the gate. Other amplification elements like the MOSFET are a bipolar junction transistor (BJT), junction field effect transistor (JFET), metal oxide semiconductor field effect transistor (MOSFET), metal semiconductor field effect transistor (MESFET), etc.

**[0044]** Hereinafter describes mostly the MOSFET among the above amplification elements. But the spirit and scope of the present invention is not limited to the

MOSFET element and may be applied all the other equivalent elements. And hereinafter describes mostly an N type MOSFET, but it is obvious to those skilled in the art that the spirit and scope of the present invention may be applied to a P type MOSFET and is not limited to the N type MOSFET.

[0045] Fig. 3 shows a circuit diagram of a variable gain LNA according to an embodiment of the present invention.

[0046] As shown in Fig. 3, the variable gain LNA according to an embodiment of the present invention comprises a first amplifying cell 3100, second amplifying cell 3300, selectively matching circuit 3500, and first means of short circuit or switch SW1. The first amplifying cell 3100 comprises a first terminal 301 and second terminal 303, and amplifies a signal applied to the first terminal 301 for high gain while minimizing additional noise in the high gain mode. The second amplifying cell 3300 comprises a first terminal 305 and second terminal 307, and amplifies a signal applied to the first terminal 305 to control the gain in the low gain mode. The selectively matching circuit 3500 comprises a first and second terminal 309, 311 and selectively changes an input impedance of the first amplifying cell 3100 for that the circuit operated in each gain mode does not act on a load respectively.

[0047] Hereinafter the connections of the LNA of Fig. 3 are described.

[0048] The first terminal 301 of the first amplifying cell 3100 is connected to the second terminal 311 of the selectively matching circuit 3500, and the second terminal 303 is connected to the second terminal 307 of the second amplifying cell 3300 and formed to an output terminal Pout of the LNA. The first terminal 305 of the second

amplifying cell 3300 is connected to the first short-circuit means or switch SW1. The first terminal 309 of the selectively matching circuit 3500 is connected to the other terminal of the first short-circuit means or switch SW1 and formed to connect to an input terminal Pin of the LNA.

**[0049]** As shown in Fig. 3, the third short-circuit terminal may be comprised between the second terminal 307 of the second amplifying cell 3300 and the output terminal Pout in the variable gain LNA according to an embodiment of the present invention. And with that structure, the output signal of the second amplifying cell 3300 outputs to the output terminal of the LNA due to the third short-circuit means or switch SW3 in the low gain mode operation.

**[0050]** Hereinafter an operation of the variable gain LNA according to an embodiment of the present invention will be described.

**[0051]** The variable gain LNA operates in two modes, a high gain mode and a low gain mode according to the power level of a received signal. That is, it operates in the high gain mode when the power level of the received signal is under a threshold of power that has been decided beforehand, and operates in the low gain mode when the power level of the received signal exceeds the threshold power.

**[0052]** The short-circuit means may reduce the signal due to having a resistance value in the state of short-circuit that can be disregarded, and may operate with a load having a finite reactance value in the open-circuit state when it is operated in the high gain mode. Accordingly, use of the short-circuit means in the circuit operated in high gain mode must be restrained, and the above load characteristics of

the short-circuit means must be carefully and respectively considered for each amplification circuit operation.

**[0053]** When it using the high gain mode, the first amplification cell 3100 is activated when the first short-circuit means SW1 is opened and HG-bias is applied to the first amplifying cell 3100. And the second amplifying cell 3300 is inert by not applying an LG-bias.

**[0054]** Accordingly, when it is operated in the high gain mode, the impedance of the second amplifying cell 3300 operated in the low gain mode does not affect the first amplifying cell 3100 operated in the high gain mode by the opening of the first short-circuit means SW1, and only the open impedance of the first short-circuit means affects the high gain mode circuit. But, the input of the first amplifying cell 3100 operated in the high gain mode is generally matched to 50 ~ 70 ohm, that is standard resistance. due to the selectively matching circuit 3500, the open impedance of the first short-circuit means SW1 has a high value of more than 50 ~ 70 ohm. So, the effect of the open impedance having a load for the first amplifying cell 3100 is ignored. Accordingly, the variable gain LNA according to an embodiment of the present invention may be the most suitable operation in high gain mode, and amplifies the input signal for a high gain.

**[0055]** When in the low gain mode, the second amplifying cell 3300 is activated by the first short-circuit means being shorted and LG-bias applied. And, the first amplifying cell 3100 is inert by not applying the HG-bias. The selectively matching circuit 3500 changes the input impedance of the first amplifying cell 3100 in the low

gain mode to a high impedance of more than the aforementioned decided value (generally standard resistance value: 50 ~ 75 ohm). Accordingly, in the low gain mode the variable gain LNA may be the most suitable operation because the first amplifying cell 3100 is not operated to bear a load of the second amplifying cell 3300 in the low gain mode.

[0056] Fig. 4 shows a circuit diagram of a variable gain LNA according to another embodiment of the present invention.

[0057] The embodiment shown in Fig. 4 is different from the variable gain LNA according to the embodiment shown in Fig. 3 in the point that a fourth short-circuit means or switch SW4 is arranged between the input terminal Pin and the output terminal Pout. The variable gain LNA according to another embodiment of the present invention directly transmits the received signal to the output terminal Pout through the fourth short-circuit means. So, power consumption may be reduced according to this embodiment. Moreover high linearity is provided and signal distortion is reduced by eliminating an input signal level of post part (normally mixer) of the variable gain LNA.

[0058] Fig. 5a shows a circuit diagram of a first amplifying cell according to an embodiment of the present invention in the variable gain LNA shown in Fig. 3 and Fig. 4.

[0059] As shown in Fig. 5a, the first amplifying cell 3100 is embodied in a common-source, and comprises an amplifying element MS51, degeneration impedance DI51, and resistor R51. The drain of the amplifying element MS51 is formed to connect to

the second terminal 303 of the first amplifying cell 3100, the gate is connected to the terminal of the resistor R51 and is formed to connect to the first terminal 301 of the first amplifying cell 3100, and the source is connected to a terminal of degeneration impedance DI51. In the other terminal of the resistor R51, when operating in the high gain mode, the first amplifying cell 3100 is activated by HG-biasing voltage, and the other terminal of degeneration impedance DI51 is grounded. Degeneration impedance DI51 can be made to use the passive or the active elements of resistor and inductor, etc.

**[0060]**As mentioned above, the common-source amplifier has excellent noise and gain characteristics, and can get satisfying input power and noise matching results at the same time, through the degeneration impedance DI51 connected to the source of the amplifying element MS51. Also, as shown in Fig. 3, the common-source amplifier can display the capability of the best suited circuit for the noise and gain sides because the matching circuit 3500 is connected to the first terminal of the first amplifying cell 3100. Therefore, when the low noise amplifier is used with the above common-source amplifier in the high gain mode which needs a high gain amplifying operation, it can display its utmost capabilities.

**[0061]**Fig. 5b is a circuit diagram for showing the inside structure of the second amplifying cell 3300 in accordance with an embodiment of the present invention in the variable gain low noise amplifier shown in Fig. 3 or Fig. 4.

**[0062]**As shown in Fig. 5b, the second amplifying cell 3300 is embodied in a common-gate, and comprises an amplifying part 510 and gain part 530.

**[0063]** The amplifying part 510 of the second amplifying cell 3300 comprises the first amplifying element MG51. The drain of the first amplifying element MG51 is connected to the connecting point of the source of the second and third amplifying element MG52, MG53 of the variable gain part, and when operating in the low gain mode, LG-biasing voltage that activates the second amplifying cell 3300 is driven, and the source is formed at the first terminal 305 of the second amplifying cell 3300.

**[0064]** In a variable gain low noise amplifier in accordance with an embodiment of the present invention, preferably, the current source (not shown, please refer to Fig. 2) is provided between the source of the first amplifying element MG51 and ground. In this case, it can change trans-conductance (gm) data of the first amplifying element MG51, and it can control input impedance data of the amplifying part 510, by control of the current source data.

**[0065]** A variable gain part 530 comprises the second and the third amplifying elements MG52, MG53 and voltage source V51 and variable voltage source V52. The drain of the second amplifying element MG52 is formed to connect to the second terminal 307 of the second amplifying cell 3300, and gate is connected to one terminal of the voltage source V51, and the source is connected to the third amplifying element MG53. The drain of the third amplifying element MG53 is connected to the power source VDD, the gate is connected to the variable voltage source V52. The drain of the third amplifying element MG53 is connected to the power source VDD, and gate is connected to variable voltage source V52.

**[0066]** An amplifying part 510 comprises the first amplifying element MG51

connected to a common-gate, and amplifies the signal driven in the first terminal 305 of the second amplifying cell 3300. As mentioned above, the common-gate amplifier can easily controlled input matching, and it has excellent linearity.

[0067]As the variable gain part 530 controls the current quantities which divide the current coming from the amplifying part into the second and the third amplifying elements MG52, MG53, by the control of the variable voltage source V52, the variable gain part 530 can vary the output coming from the second terminal 307 of the second amplifying cell 3300, and it can control in succession the gain data of the second amplifying cell 3300. In addition, because the current of the first amplifying element MG51 is not changed by the variable gain part 530, the trans-conductance data of the first amplifying element MG51 is regular, the input matching of the second amplifying cell 3300 is not changed.

[0068]Therefore, if the variable gain part is used in the second amplifying cell 3300, which has common-gate construction shown in Fig. 5b, in the low gain mode, it can perform successive variable gain functions without changing the characteristic of the input matching, and a low noise amplifier can be provided with excellent linearity.

[0069]Fig. 5c is a circuit diagram for showing a selective matching circuit 3500 in accordance with an embodiment of the present invention for the variable gain low noise amplifier shown in Fig. 3 or Fig. 4.

[0070]As shown in Fig. 5c, the selective matching circuit 3500 in accordance with an embodiment of the present invention comprises the first and the second inductors L51, L52 and capacitor C51 and the second short circuit-means or switch SW2.

**[0071]** One of the terminals of the first inductor L51 is connected to the second inductor L52 and capacitor C51, the other terminal is connected to one of the terminals of the second short circuit-means SW2. The other terminal of the second inductor L52 is formed to connect to the first terminal 309 of the selective matching circuit 3500, the other terminal of the capacitor C51 is formed to connect to the second terminal 311 of the selective matching circuit 3500, the other terminal of the second short circuit-means SW2 is grounded.

**[0072]** In the selective matching circuit 3500 in accordance with an embodiment of the present invention, the second short circuit-means SW2 can display the capability of the best suited circuit in a state in which the first amplifying cell 3300 is activated by high gain mode driven HG-biasing; in case of low gain mode, i.e., HG-biasing is not driven, the selective matching circuit 3500 is selected to have an input impedance of the high gain mode circuit block which is made by selective matching circuit 3500 and the first amplifying cell 3100, in case the first amplifying cell 3100 is not activated.

**[0073]** Fig. 6a shows a circuit diagram of the variable gain low noise amplifier shown in Fig. 3 using circuits shown in Fig 5a, 5b, and 5c.

**[0074]** As shown in Fig 6a, a variable gain low noise amplifier in accordance with an embodiment of the present invention comprises the first and second amplifying cells 3100, 3300, the selective matching circuit 3500, and the first short circuit-means or switch SW1.

**[0075]** The first amplifying cell 3100 is embodied in the form of a common-source

and is operated in the high gain mode, and the second amplifying cell 3300 is embodied in the form of a common-gate and is operated in the low gain mode. Moreover, the selective matching circuit 3500 comprises the second short circuit-means, and in high gain mode, the input of the first amplifying cell 3100 is matched by the selective matching circuit 3500 in order that the first amplifying cell 3100 can display the capability of the best suited circuit; and in the low gain mode, the input impedance of the first amplifying cell 3100 is changed to a high data mode by the selective matching circuit 3500, and the first amplifying cell 3100 is not operated using the load of the second amplifying cell 3300. Therefore, the variable gain low noise amplifier in accordance with an embodiment of the present invention can display the capability of the best suited circuit in each gain mode.

**[0076]**Also, a variable gain low noise amplifier in accordance with an embodiment of the present invention uses with a common-source the first amplifying cell 3100 in the high gain mode that demands high noise and gain characteristics, and uses a common-gate with the second amplifying cell 3100 in the low gain mode that demands high linearity and successive variable gain, as a consequence of that, linearity is good, input matching is easy, and the amplifier can have a variable gain low noise amplifier with possible successive variable gain functions.

**[0077]**Furthermore, in case the power level of the receiving signal is enough large and amplifying is not needed because the receiving signal is directly passed to the output terminal by the fourth short circuit-means or switch SW4 shown in Fig. 4 , power consumption that is demanded for the amplifying operation is not needed.

[0078] Fig.6b and Fig. 6c are circuit diagrams shown in equivalent input parts of the first amplifying cell 3100 in order to describe more specifically the operation of the selective matching circuit 3500 in accordance with an embodiment of the present invention in the case a variable gain low noise amplifier is operated in the high gain mode or the low gain mode.

[0079] In the high gain mode, the second short circuit-means is open, and the input activating the first amplifying cell 3100 can be shown in a equivalent ZHG, on. At this time, the variable gain low noise amplifier can be gotten the capability of the best suited circuit by matching the input impedance of the first amplifying cell 3100 by using the second inductor L52 and capacitor C51. That is, because the electric powers of the variable gain low noise amplifier and the first amplifying cell 3100, the high gain mode characteristic of the best suited circuit can be realized.

[0080] In the low gain mode, the second short circuit-means is short, and inactivating the input of the first amplifying cell 3100 can be shown in a equivalent ZLG, off. Here, ZLG, off as shown in the views is very different from the ZHG, on data; in this case, the matching circuit 3500 comprises the first and the second inductor L51, L52 and capacitor C51. The first inductor L51 handles inductance data that are sent to the input part of the first amplifying cell 3100 providing substantial infinite input impedance from the node 309. As it does in the low gain mode, the input part of the first amplifying cell 3100 is not affected by in the second amplifying cell 3300. Therefore, the input of the variable gain low noise amplifier is matched to the most suitable of input of the second amplifying cell 3300, because the maximum power

Pin is transferred, and at the same time, the power of the first amplifying cell 3100 is substantially zero, thus, variable gain low noise amplifier realizes the low gain mode characteristics of the best suited circuit.

#### INDUSTRIAL APPLICABILITY

**[0081]**In a low noise amplifier in accordance with the present invention, because the operating circuits in each gain mode is not affected by the performance of the operating circuit of the best suited circuit of the other gain mode, the each circuit can display the capability best suited to each mode.

**[0082]**Also, input matching, gain, noise characteristic and linearity etc, can display the capability best suited to each other in different gain modes.

**[0083]**Further, each circuit operates in a gain mode with at least two according to the size of the receiving signals, and can vary gain in the low gain mode.

**[0084]**Furthermore, because the output of each circuit can equal the receiving signals by the short circuit-means, amplifying operation is not needed, and the power consumption is reduced.